



# Spartan<sup>®</sup>-II Evaluation Kit

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## Xilinx Spartan® -II Evaluation Kit

### Kit Features

- FPGA
  - Xilinx® Spartan-II XC2S150-5PQ208 or XC2S150-5PQ208
- SPROM
  - Xilinx® XC18V01SO20C
- Board I/O Connectors
  - Two 50-pin, 0.1 Header connector
  - Pads for three MICTOR connectors
  - Pads for one 140 pin General Purpose I/O interface
- Power
  - +5.0 Power Connector
  - +3.3 V Regulated Supply
  - +2.5 V Regulated Supply
  - Full Bypass Capacitance
- Communication
  - RS232 Serial Port
- Configuration
  - JTAG Header Connector
  - In-System Programmable PROM
- Miscellaneous
  - 8 DIP switches
  - 2 Push-buttons,
  - 8 LEDs
  - 40 MHz Oscillator
  - Digital Thermometer
- Demonstration application (Source VHDL)
  - Simple RS232
  - Digital Thermometer
  - LED Patterns

### Description

The Spartan-II Evaluation Kit is used by engineers as a platform to test FPGA designs that are targeted to the Xilinx Spartan-II device. It is also a

great tool for beginners to get acquainted with FPGAs and VHDL.

The Spartan-II device is located in the center of the board. It can be configured via a JTAG download or from the on board configuration PROM. The configuration PROM is also programmable through the JTAG cable. Over 85 IO signals are connected from the FPGA to 0.1 header connectors for user connections. Other I/Os are connected to 8 LED, 8 DIP-switches, two push buttons, RS-232 line driver/receiver, and a digital thermometer.



### Demo Application

The Kit is supplied with complete VHDL source code that:

- 1) Sequences LEDs
- 2) Reads Dip Switches/push buttons
- 3) Senses Temperature and displays bit value on LEDs
- 4) Transmits startup message through RS-232 connector.
- 5) Echoes RS-232 commands. (Serial cable not included)

### Ordering Information

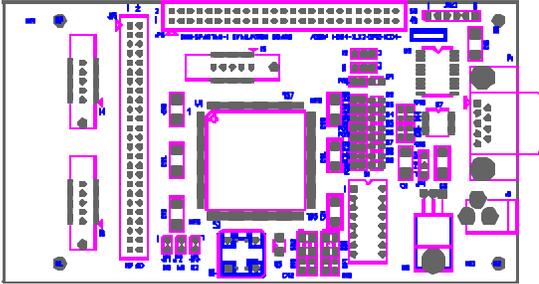
The following table lists the evaluation kit part number.

**Table 1:** Spartan-II Evaluation Kit

Part Number	Hardware
<a href="#">ADS-XLX-SP2-EVL</a>	Xilinx Spartan-II Evaluation Kit

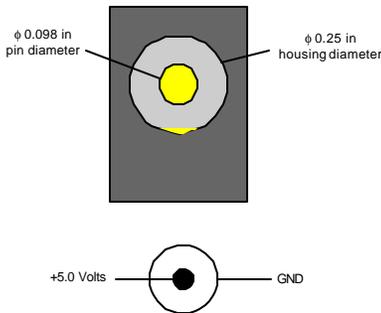
## Spartan-II Evaluation Kit

This section provides information basic to the design of the Spartan-II evaluation board.



### Power

The majority of the design is powered at 3.3V with the Spartan-II FPGA core powered at 2.5V. The board should be powered by a 5-volt bench supply. The 3.3V is derived via a linear regulator. A linear regulator from the 3.3V provides the 2.5V Xilinx core voltage. A barrel connector J3 (RAPC712) is provided on the board for lab supply connections. The center tap is +5.0 volts and the outer is GND. Note: The lab supply should be regulated at 5.0 volts. While current requirements are dependent on the user application, it is suggested to limit the supply to 1.5 amps on initial power up.



### Printed Circuit Board

The Evaluation Spartan-II Kit printed circuit board is a 6-layer board with four signal layers, a full 3.3V power plane incorporating an isolated 2.5V mini-plane, and full ground plane. The board stack-up layers 1 through 6 is:

- 1) "Component side"/signal
- 2) Ground Plane
- 3) Signal
- 4) Signal
- 5) Power: 3.3V and 2.5V
- 6) "Solder side"/signal

## Spartan-II FPGA

The Spartan-II Field-Programmable Gate Array device (U1) utilized in this design is the 100+K-system gate device (XCV100) or the 150+K-system gate device (XCV150) in a PQ208 package.

### FPGA Configuration

Configuration information is provided from two sources; the JTAG Connector (JTAG0), and configuration PROM.

**Table 2:** JTAG Connector

Signal Name	JTAG Connector Pin #
VCC	1
TDI	2
TMS	3
TCK	4
TDO	5
GND	6

Jumpers JP1, JP2 and JP3 select the configuration mode of the Spartan. The following table shows the jumper setting needed for each mode.

**Table 3:** Mode Select

Configuration Mode	Pull-ups	JP3/M2	JP2/M1	JP1/M0
Master-serial	No	OFF /LOW	OFF /LOW	OFF /LOW
Boundary-scan	No	ON /HIGH	OFF /LOW	ON /HIGH
SelectMAP	No	ON /HIGH	ON /HIGH	OFF /LOW
Slave-serial	No	ON /HIGH	ON /HIGH	ON /HIGH
Master-serial	Yes	ON /HIGH	OFF /LOW	OFF /LOW
Boundary-scan	Yes	OFF /LOW	OFF /LOW	ON /HIGH
SelectMAP	Yes	OFF /LOW	ON /HIGH	OFF /LOW
Slave-serial	Yes	OFF /LOW	ON /HIGH	ON /HIGH

The LED D1 indicates the output level of the DONE pin of the Spartan-II device. It will illuminate when the Spartan-II configuration is complete.

### System Clock

An oscillator socket clock output is connected to the Spartan-II device. U6 is connected to Global Clock

Input #0 (PQ208 pin #P80), The U6 socket is populated with a 40 MHz oscillator.

### Asynchronous (RS232) Communication Interface

The ADM3222 device provides level translation for a single RS232 interface (DB9 connector). The second translation port on the device is terminated and unused.

**Table 4:** RS-232 Interface Signals

RS232 SIGNAL	Spartan-II PIN #
R1OUT	P152
T1IN	P151
EN_N	P150
SD_N	P149

**Table 5:** RS-232 Connector Pinout

Signal Name	P2 (DB9) connector Pin #
TX out	2
RX in	3
GND	5

### Miscellaneous

The “Miscellaneous” interfaces on the Spartan-II™ board consist of a single 8-position DIP-switch (8-individual SPST switches), 8 LEDs, and two push-button switches.

**Table 6:** DIP-Switch Signals

DIP SW	Spartan-II PIN #
#1	P123
#2	P122
#3	P121
#4	P120
#5	P114
#6	P113
#7	P112
#8	P111

**Table 7:** Push Button Switch Signals

BUTTO N	Spartan-II PIN #
SW1	P110
SW2	P109

**Table 8:** LED Control Signals

LED	Spartan-II PIN #
D2	P141
D3	P140
D4	P139
D5	P138
D6	P136
D7	P134
D8	P133
D9	P132

**Table 9:** Digital Thermometer

LED	Virtex-E PIN #
CE	P96
SCLK	P97
SDI	P95
SDO	P94

## I/O Signal Headers

Two 50-pin connectors provide 84 Spartan-II I/O lines and 6 ground pins.

**Table 10:** GPIO Signals JP5

GPIO CONNECTOR PIN #	Spartan-II PIN #
1	P3
2	P4
3	P5
4	P6
5	P7
6	P8
7	P9
8	P10
9	P14
10	P15
11	P16
12	P17
13	P18
14	P20
15	P21
16	P22
17	P23
18	P24
19	P27
20	P29
21	P30
22	P31
23	P33
24	P34
25	P35
26	P36
27	P37
28	P41
29	P42
30	P43
31	P44
32	P45
33	P57
34	P58
35	P59
36	P60
37	P61
38	P62
39	P63
40	P67
41	P68
42	P69
43	P70
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	GND
49	GND
50	GND

**Table 11:** GPIO Signals JP6

GPIO CONNECTOR PIN #	Spartan-II PIN #
1	P206
2	P205
3	P204
4	P203
5	P202
6	P201
7	P200
8	P199
9	P195
10	P194
11	P193
12	P192
13	P191
14	P189
15	P188
16	P187
17	P181
18	P180
19	P179
20	P178
21	P176
22	P175
23	P174
24	P173
25	P172
26	P168
27	P167
28	P166
29	P165
30	P164
31	P163
32	P162
33	P71
34	P73
35	P74
36	P75
37	P81
38	P82
39	P83
40	P84
41	P86
42	P87
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	GND
49	GND
50	GND

## Logic Analyzer Connector

Three AMP™ MICTOR connector pads are provided to connect to a logic analyzer's mass termination cable.

**Table 12: MICTOR J4**

Connector PIN #	Spartan-II PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P182*	CLK_OUT
6	P80	OSC
7	P45	ADDRESS31
8	P22	ADDRESS15
9	P44	ADDRESS30
10	P21	ADDRESS14
11	P43	ADDRESS29
12	P20	ADDRESS13
13	P42	ADDRESS28
14	P18	ADDRESS12
15	P41	ADDRESS27
16	P17	ADDRESS11
17	P37	ADDRESS26
18	P16	ADDRESS10
19	P36	ADDRESS25
20	P15	ADDRESS9
21	P35	ADDRESS24
22	P14	ADDRESS8
23	P34	ADDRESS23
24	P10	ADDRESS7
25	P33	ADDRESS22
26	P9	ADDRESS6
27	P31	ADDRESS21
28	P8	ADDRESS5
29	P30	ADDRESS20
30	P7	ADDRESS4
31	P29	ADDRESS19
32	P6	ADDRESS3
33	P27	ADDRESS18
34	P5	ADDRESS2
35	P24	ADDRESS17
36	P4	ADDRESS1
37	P23	ADDRESS16
38	P3	ADDRESS0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

**Table 13: MICTOR J5**

Connector PIN #	Spartan-II PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P185*	GCK3
6	P77*	GCLK1
7	P162	DATA31
8	P187	DATA15
9	P163	DATA30
10	P188	DATA14
11	P164	DATA29
12	P189	DATA13
13	P165	DATA28
14	P191	DATA12
15	P166	DATA27
16	P192	DATA11
17	P167	DATA26
18	P193	DATA10
19	P168	DATA25
20	P194	DATA9
21	P172	DATA24
22	P195	DATA8
23	P173	DATA23
24	P199	DATA7
25	P174	DATA22
26	P200	DATA6
27	P175	DATA21
28	P201	DATA5
29	P176	DATA20
30	P202	DATA4
31	P178	DATA19
32	P203	DATA3
33	P179	DATA18
34	P204	DATA2
35	P180	DATA17
36	P205	DATA1
37	P181	DATA16
38	P206	DATA0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

**Table 14: MICTOR J6**

Connector PIN #	Spartan-II PIN #	Name
1	N/C	N/C
2	N/C	N/C
3	N/C	N/C
4	N/C	N/C
5	P182*	CLK_OUT
6	P147*	CLK_IN
7	P154	DOUT
8	P81	CNTL15
9	P109	SWITCH9
10	P75	CNTL14
11	P110	SWITCH8
12	P74	CNTL13
13	P94	TEMP_SDO
14	P73	CNTL12
15	P95	TEMP_SDI
16	P71	CNTL11
17	P96	TEMP_CE
18	P70	CNTL10
19	P97	TEMP_SCLK
20	P69	CNTL9
21	P149	RS232SD_N
22	P68	CNTL8
23	P150	RS232EN_N
24	P67	CNTL7
25	P151	RS232TX
26	P63	CNTL6
27	P152	RS232RX
28	P62	CNTL5
29	P87	CNTL20
30	P61	CNTL4
31	P86	CNTL19
32	P60	CNTL3
33	P84	CNTL18
34	P59	CNTL2
35	P83	CNTL17
36	P58	CNTL1
37	P82	CNTL16
38	P57	CNTL0
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND

\*Note: A zero ohm resistor may be required to access the noted signals.

**AvBus Connector**

A high-density connector pads are located on bottom of the board. The signals are listed in the following table.

**Table 15: AvBus Connector P2**

Name	FPGA PIN #	Connector PIN #	FPGA PIN #	Name
ADDRESS0	P3	71	1	N/C
GND	GND	72	2	P4
ADDRESS3	P6	73	3	P5
ADDRESS4	P7	74	4	GND
GND	GND	75	5	P8
ADDRESS7	P10	76	6	P9
ADDRESS8	P14	77	7	GND
AUX_+3.3V	+3.3V	78	8	P15
ADDRESS11	P17	79	9	P16
ADDRESS12	P18	80	10	GND
GND	GND	81	11	P20
ADDRESS15	P22	82	12	P21
ADDRESS16	P23	83	13	N/C
GND	GND	84	14	P24
ADDRESS19	P29	85	15	P27
ADDRESS20	P30	86	16	GND
GND	GND	87	17	P31
ADDRESS23	P34	88	18	P33
ADDRESS24	P35	89	19	GND
AUX_+3.3V	+3.3V	90	20	P36
ADDRESS27	P41	91	21	P37
ADDRESS28	P42	92	22	GND
GND	GND	93	23	P43
ADDRESS31	P45	94	24	P44
DATA0	P206	95	25	N/C
GND	GND	96	26	P205
DATA3	P203	97	27	P204
DATA4	P202	98	28	GND
GND	GND	99	29	P201
DATA7	P199	100	30	P200
DATA8	P195	101	31	GND
AUX_+3.3V	+3.3V	102	32	P194
DATA11	P192	103	33	P193
DATA12	P191	104	34	GND
GND	GND	105	35	P189
DATA15	P187	106	36	P188
DATA16	P181	107	37	N/C
GND	GND	108	38	P180
DATA19	P178	109	39	P179
DATA20	P176	110	40	GND
GND	GND	111	41	P175
DATA23	P173	112	42	P174
DATA24	P172	113	43	GND
AUX_+3.3V	+3.3V	114	44	P168
DATA27	P166	115	45	P167
DATA28	P165	116	46	GND
GND	GND	117	47	P164
DATA31	P162	118	48	P163
CNTL0	P57	119	49	N/C
GND	GND	120	50	P58
CNTL3	P60	121	51	P59
CNTL4	P61	122	52	GND
GND	GND	123	53	P62
CNTL7	P67	124	54	P63
CNTL8	P68	125	55	GND

Name	FPGA PIN #	Connector PIN #	FPGA PIN #	Name
AUX_+3.3V	+3.3V	126	56	P69 CNTL9
CNTL11	P71	127	57	P70 CNTL10
CNTL12	P73	128	58	GND GND
GND	GND	129	59	P74 CNTL13
CNTL15	P81	130	60	P75 CNTL14
CNTL16	P82	131	61	N/C N/C
GND	GND	132	62	P83 CNTL17
CNTL19	P86	133	63	P84 CNTL18
CNTL20	P87	134	64	GND GND
GND	GND	135	65	P147* CLK_IN
CLK_OUT	P182*	136	66	P182* CLK_OUT_F B
TMS	⊕	137	67	GND GND
AUX_+3.3V	+3.3V	138	68	⊕ TDO
TDI	⊕	139	69	⊕ TCK
TRS	⊕	140	70	GND GND

\*Note: A zero ohm resistor may be required to access the noted signals.

⊕Note: Reference Schematic for current JTAG signal paths.

## Demonstration Code

Supplied with the Evaluation Kit is a demonstration program file that utilizes several devices on the evaluation board. The demonstration program uses the evaluation board as a standalone platform that is connected to a lab supply and a terminal emulation program. On power up the FPGA will be configured by the onboard PROM. Upon completion of the configuration the FPGA functionality and input/output signal will activate. A start up serial message will be sent to the terminal port via the RS-232 connection. The LEDs will display a back and forth scanning pattern or 8-bit value corresponding to the current temperature.

### Additional Items Needed:

- Lab power supply, 5.0 volts at 1.5 amps.
- Serial Terminal or Terminal Emulator.
- RS-232 cable

### Setup:

- 1) Attach the lab supply to the power connector on the Evaluation Board.
- 2) Attach the serial terminal to the P1 connector of the Evaluation Board.
- 3) Set the Serial Terminal to: 8 data bits, 1 stop, No parity, 9600 baud.
- 4) Verify jumper are NOT installed on JP1,JP2,and JP3.
- 5) Verify JP4 is installed across pins 1 and 2.

### Power UP:

- 6) Apply power to the Evaluation Board.

- 7) The DONE LED D1 will light on the completion of the download.

### Reset:

- 8) Press the Soft Reset button SW1 to reset the board.

### Serial Demo

- 9) Press the button SW2 to send the startup message.
- 10) The Power up message is displayed on the serial terminal.
- 11) All characters typed should be echoed to the terminal.
- 12) Press the Reset button again to “reset” startup message.

### LED SCAN

- 13) Set the dipswitch S1 dip 1 to ON (rocker up).
- 14) The LEDs should be blinking such that the illuminated led should be scanning back and forth through the LED array.

### TEMPERATURE

- 15) Set the dipswitch S1 dip 1 to OFF (rocker down).
- 16) The LED should now display the temperature in °C in two's complement binary. See the following table.
- 17) Hold your finger on U5 to change the temperature.

LED Pattern (D9..D2)	Decimal Value (°C)
0111 1000	+120C
0001 1001	+25C
0000 1010	+10C
0000 0000	0C
1111 0101	-10C
1110 0110	-25C
1100 1001	-55C

## Relevant Documents

Documents relevant to this application are listed in the following table.

**Table 16:** Relevant Documents and Links

Document	Source
XILINX SPARTAN-II FPGA Data Sheet	<a href="http://www.xilinx.com/partinfo/ds001.pdf">http://www.xilinx.com/partinfo/ds001.pdf</a>
XILINX XC18V01 Configuration PROM Data Sheet	<a href="http://www.xilinx.com/partinfo/ds026.pdf">http://www.xilinx.com/partinfo/ds026.pdf</a>
Analog Devices ADM3222 3V RS232 Line Driver/Receiver Data Sheet	<a href="http://www.analog.com/pdf/ADM3202_0.pdf">http://www.analog.com/pdf/ADM3202_0.pdf</a>

# Block Diagram

